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(54) Apparatus and method for statistical eye diagram measurement of a serial bit stream

(57) Disclosed herein is an apparatus and a method for determining characteristics of a bit stream of binary pulses having measuring apparatus for sampling pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream. Control apparatus coupled to the measuring apparatus generates a series of the threshold voltage levels and the delayed clock pulses during each period of a bit stream pulse. Multipl counts of the sampled pulse voltage levels are recorded during each delayed clock pulse and accumulated for a series of pulses of the binary coded pulse bit stream. The control apparatus analyzes and processes the accumulated counts to generate an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

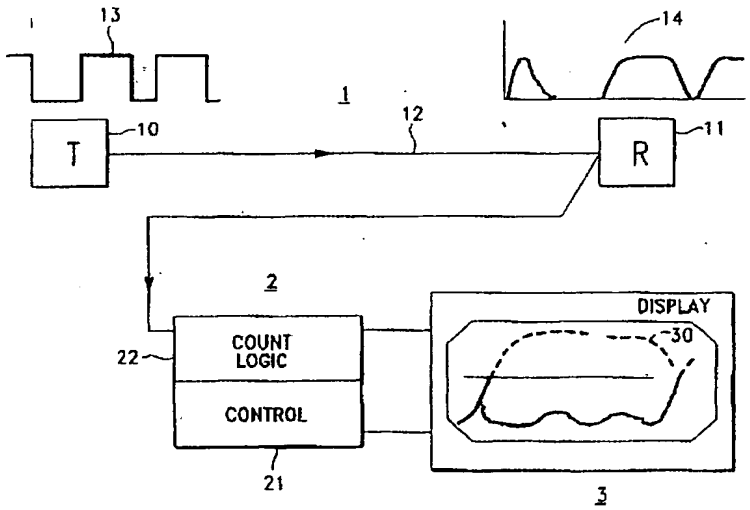

FIG.—1

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Description

[0001] This invention relat s to apparatus and a method for analyzing a waveform and in particular to apparatus and method for the statistical eye diagram measurement of a high speed binary pulse coded bit stream.

[0002] High-speed communication systems typically communicate with each other by sending serial bit streams of data between transmitters and receivers. These bit streams are usually binary coded pulse signals represented by zeros and ones which may be electrical voltages or optical signals derived from the electrical voltages created by the transmitters and which pulse coded signals are applied to a transmission facility connecting the transmitters with the receivers. The receivers decode the received pulse code signal data to obtain the information therein.

[0003] If a receiver receives pulse code signals that have been deformed by errors occurring in the transmission facility problems or if the receiver improperly decodes the received pulse coded signals, the effect is that bit errors may occur in the communications there resulting in wrong information being received by the receiver. Thus, designers, engineers, installers and maintenance personal need to evaluate the stream of pulse coded signals, oftentimes called bit streams, to monitor system performance and to help in diagnosing system problems. It is typical to monitor the quality of such bit streams by using a sampling oscilloscope.

[0004] In the monitoring operation, the bit stream and a trigger input in form of a clock signal having a repetition rate identical to the repetition rate of the bit stream and synchronous therewith are applied to the inputs of the sampling oscilloscope. Samples of the voltage levels of the binary pulses of the bit stream are taken at various time offsets from the repetitive trigger input and are plotted as sample points on the display of the oscilloscope. Voltage samples are continuously taken of the bit stream and added to the sample oscilloscope in combination with the older sample points, which continue to exist on the sample oscilloscope display. Over a relatively short period of time, hundreds or thousands of the sample points on the sample oscilloscope display plot the possible voltage distributions at each time offset from the trigger input. By sweeping all time offsets in the range of interest, a diagram appears on the sampling oscilloscope display, which reveals the quality of the measured high-speed bit stream. This type of diagram, oftentimes called an "eye" diagram, is often used to view high speed binary pulse bit streams during the various development, installation and maintenance phases of high-speed communications systems.

[0005] A problem exists in using sampling oscilloscopes in this manner to measure the quality of high-speed communication systems. As the bit stream data rat increases, the bandwidth of th sampling oscilloscop s ne ded to create the y diagrams increases proportionally there resulting in a higher cost.

[0006] Another problem arises in that as the cost of th sampling oscilloscopes increases and due to the design issues of super high-speed systems, the present sampling methods takes samples at a relatively few of all the possible edges of th bit stream puls s thereby limiting the current effective sampling rate in the range of ten thousand samples per second by typical known systems. Accordingly, a need exists in the art for apparatus and a method for actively determining the quality of high-speed binary pulse bit streams used to transfer information and data between communications systems.

[0007] It is an object of the invention to provide binary pulse coded waveform measuring apparatus for determining the characteristics of a high speed bit stream of binary pulses used to transfer information between communications systems and in particular to generate an eye diagram defining the quality of the binary pulse bit stream.

[0008] It is also an object of the invention to provide to provide logic apparatus for sampling pulse voltag levels in excess of a series of voltage threshold levels during each of a series of delayed clock pulses for a series of pulses of the binary pulse bit stream.

[0009] It is also an object of the invention to provide control apparatus coupled to the logic apparatus and controlled by a programmed processor to generate the series of the threshold voltage levels and the delayed clock pulses during each period of a bit stream pulse.

[0010] The control apparatus accumulates multipl counts of the sampled pulse voltage levels during each delayed clock pulse for a series of pulses of the binary coded pulse bit stream and processes the accumulated counts to generate an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

[0011] It is a further object of the invention to provide a method for determining characteristics of a bit stream of binary pulses by sampling pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream. The method generates a series of th voltage threshold levels and the delayed clock pulses during each period of a bit stream pulse and accumulating multiple counts of the sampled pulse voltage levels during each delayed clock pulse for a series of pulses of the binary pulse bit stream. The accumulated counts are processed to generate an eye diagram defining the characteristics of the binary pulse bit stream.

[0012] In a preferred embodiment of the invention, apparatus for determining characteristics of a bit stream of binary pulses has measuring apparatus for sampling pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream. Control means coupled to the measuring apparatus generates a series of the threshold voltage levels and the delayed clock pulses during each period of a bit stream puls and accumulat s multipl counts of th sampled pulse voltag

levels during each delayed clock pulse for a series of pulses of the binary coded pulse bit stream. The accumulated counts are processed to generate an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

[0013] Also in accordance with the preferred embodiment of the invention, a method for determining characteristics of a bit stream of binary pulses generates a series of threshold voltage levels and delayed clock pulses during each period of a bit stream pulse. The method steps measures and accumulates multiple counts of pulse voltage levels in excess of the generated voltage threshold levels during each delayed clock pulse for a series of pulses of the binary coded pulse bit stream. The method then analyzes processes the accumulated voltage counts and generates an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

[0014] For a further understanding of the objects and advantages of the present invention, reference should be had to the following detailed description, taken in conjunction with the accompanying drawing figures, in which like parts are given like reference numerals and wherein:

Fig. 1 is a block diagram of binary pulse coded waveform measuring apparatus in accordance with the principles of the invention connected to a communication system for generating a statistical eye diagram measurement of a binary pulse coded waveform transmitted from a system transmitter to a system receiver,

Fig. 2 is a block diagram of the binary pulse coded waveform measuring apparatus set forth in Fig. 1,

Fig. 3 is a flow chart of the operation of the measuring apparatus set forth in Figs. 1 and 2 for generating an array of data counts of the measurement of the voltage levels versus time of each pulse of the high speed binary bit stream set transmitted between the transmitter and receiver of the communication system set forth in Fig. 1,

Fig. 4 is a flow chart of the operation of the measuring apparatus set forth in Figs. 1 and 2 for processing the measurement data generated by the flow chart of Fig. 3 into a statistical array of eye diagram data,

Fig. 5 is an example representation of the raw sample count data processed by operation of the measurement algorithm flow chart of flow chart of Fig. 3, and

Fig. 6 is an example representation of the statistical data processed by the operation of the processing algorithm flow chart of flow chart of Fig. 5 to form an eye diagram representing the characteristics and quality of the high speed binary bit stream transmitted between the transmitter and receiver of the communication system set forth in Fig. 1.

[0015] Referring to Fig. 1 of the drawing, high-speed communication system 1 consists of a transmitter 10 interconnected by a transmission facility 12 with a receiver 11. Information is transmitted to receiver 11 in a binary coded pulse format as a binary bit stream 13 applied to the input of transmission facility 12. Transmission facility 12 may be any one of a large number of high-speed transmission facilities such as coaxial cables, optical fibers, radio and satellite links or the like. In a typical application, the binary pulses of input binary bit stream 13 may be reconfigured by the characteristics of the transmission facility 12 and appear as the rounded binary coded pulse format shown as the binary bit stream 14 received by receiver 11. The binary pulse coded waveform measuring apparatus 2 as set forth in Fig. 1, may be connected to transmission facility 12 at either the output of transmitter 10, the input of receiver 11, at various locations along transmission facility 12 or at various locations within transmitter 10 and receiver 11 wherein it is desired to measure the quality of the transmitted and received binary pulse coded bit streams. In operation, control 21 controls the operation of count logic 20 to generate a statistical eye diagram 30 representing the quality of the measured the binary pulse coded bit stream 14 on display apparatus 3 which may be any one of a number of well known display such as a computer or stand alone monitors, plotters, various storage devices, or the like.

[0016] In order to create an eye diagram from the measured high speed pulse coded bit stream, samples must be collected from the waveform such that the samples correspond to the number of times that the waveform of the measured pulse crosses over a time offset and voltage coordinate for all the time offsets and voltage levels of interest. In general, a pulse coded bit stream consists of a series of succeeding "0" and "1" pulses wherein each "0" pulse is transmitted at one voltage level and each "1" pulse is transmitted at another voltage level. The specific sequence of the of the "0" and "1" pulses define the information or data transmitted by transmitter 10 to receiver 11. The pulses have a repetition rate wherein each pulse has a period of time, hereinafter referred to as the pulse period, and follows a preceding pulse at the repetition rate determined by the communication system clock.

[0017] Measuring apparatus, or count logic 20, controlled by control 21, samples the pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream. Count logic 20 collects counts of the voltage of each pulse during the pulse period at variable voltage thresholds VVT occurring at voltage steps (V between a minimum voltage VMIN and a max-

imum voltag VMAX at a variable time delayed clock pulse TVD occurring in time steps (T betw en a rang of z ro and a s l ct d maximum time TMAX. Control 21 coupled to the count logic 20 generates a series of the threshold voltage levels VVT and th delayed clock pulses TVD during each period of a bit stream pulse and accumulates multiple counts of the sampled pulse voltage levels in excess of the threshold voltage levels VVT during each delayed clock pulse TVD for a series of pulses of the binary coded pulse bit stream. The counts are recorded by control 21 as an Eye Data Array A1 2111 in memory 211 wherein the count data is stored at positions TVD, VVT in the array defined by the voltage threshold levels VVT separated by the voltage step (V and at ones of the delayed clock pulses TVD separated by the time step (T during pulse periods of the series of pulses succeeding the first measured binary pulse. Thus, the count starts in each pulse at time zero of the pulse period wherein counts of the pulse voltage level are taken and recorded in the Eye Data Array as the variable voltage threshold VVT is moved from the minimum voltage VMIN to the maximum voltage VMAX. The time delay clock pulse TVD is advanced in time a time step (T and the counting process repeated. The count measurement continues in (T steps until time TMAX is reached. The measurement of the counts may be continued over a large number of the bit stream pulses, for example, over several thousand serial pulses, with the total count being recorded in the eye data array.

[0018] The binary pulse coded waveform measuring apparatus 2, Fig. 2, comprises count logic 20 controlled by a control 21. Control processor 21 may be any one of a number of different types of computers and need not be described in great detail. Sufficient for an understanding of the invention, control 21 has a processor 210 connected by a bus 212 to a memory 211 and a display unit 3. Processor 210 is also connected by bus 212 to address registers 213 and 215, the operation of the registers are well known. In the general operation, processor addresses address register 213 and requests that the count data received from the above threshold counter 202 of count logic 21 and stored in address register 213 be recorded in the eye data array A1, 2111 of memory 211. Processor 210 also addresses address registers 215 and transfers information thereto that is stored in the address registers and used to control various components in the count logic 20. The high-speed binary bit stream is applied to interface 216 so that processor 210 can generate clock pulses that are synchronous the repetition rate of the bit stream. Programs stored in memory 21 control processor 210 in the operation of the count logic 20 and control logic 21 in accordance with the principles of the invention.

[0019] Count logic 20 has a one-bit comparator 200 with one input connected to the transmission facility 12 or other point in th transmitter 10 or receiv r 11 to measure the high sp d binary coded bit stream. Th logic elements 200 and 201 are the main sampling components and are comprised of a D-type flip-flop 201 proceeded by a one-bit comparator 200. The one-bit comparator 200 will output a high when the signal voltage on the positive pin is higher than the signal voltage on th n gativ pin. The D-flip flop 201 will copy th valu on the "D" input to the "Q" output connected to the enable input of the above threshold counter 202. In operation, processor 210 determining a pulse repetition rate of the high speed binary pulse bit stream by interfac 216 and generates a series of the time delay clock pulses TVD each separated by a predefined time step (T during a period of each binary pulse and applies the time delay clock pulses TVD to the above threshold count r 202 and measurement window counter 203 via and address register 215. The above threshold counter 202 is a synchronous enableable and resetable counter and is of a type well known in the art. The counter will increment when not reset only when the enable line is "1" (high) at the rising edge of a clocking signal applied to the counter. Above threshold counter 202 holds the number of counts that succeeded in being higher then the voltage threshold VVT as the voltage threshold VVT is moved from the minimum voltage VMIN to the maximum voltage VMAX. threshold at the time of the rising edge of the time delay clock pulse TVD. The measur ment window counter 203 is also a synchronous enableable and resetable counter and sets the measurement window size which sets the number of bits that are looked at to compute the "Above Threshold" count for each time delay clock pulse TVD and voltage threshold VVT position in the eye diagram. The variable voltage threshold VVT is a static control voltage applied to the negative pin of comparator 200 and is set by processor 210 by addressing address register 215 to control the digital to VVT converter 214 to step this voltage in pr cise increments and apply the appropriate voltage step (V increment to the negative pin of comparator 200.

[0020] Control 21 initiates the start sample sequenc by applying a start pulse to reset the above threshold counter 202 and measurement counter 203 which start accumulating data. Once the measurement window counter 203 reaches it's terminal count, the apparatus will automatically stop and hold with the current "Abov Threshold" count ready to be stored away. To start the next measurement, control 21 generates a new variabl voltage threshold VVT and/or variable time delay clock pulse TVD and another start pulse.

[0021] The measurement algorithm, Fig. 3, is stored in memory 211 and starts controlling control 1 to apply the start pulse to control logic 20. The initial value of the variable time delay pulse TVD is set to zero, step 21110, and values selected by the user are assigned to tim TMAX, voltage VMAX, time step (T, voltage step (V and minimum voltage VMIN, step 21111. If the value of time delay pulse TVD is greater than the value of time TMAX, step 21112, the algorithm is compl ted. If not, the variabl voltage threshold VVT is s t to th value of minimum voltage VMIN, step 21113. Count logic 20 takes

the count, step 21114, and records the count in eye diagram array (EDA) Al 2111 at the position EDA (time delay pulse TVD, variable voltage thr shold VVT), step 21115. The variable voltage threshold VVT is increased by the valu of the voltage st p (V. If the new valu of the variable voltage threshold VVT, step 21117, is less than the value of voltage VMAX, the algorithm repeats steps 21114 through 21116 to record counts in the eye data array 2111 at the appropriate time delay pulse TVD and variable voltage threshold VVT array positions. When the value of the variable voltage threshold VVT becomes greater than the value of the voltage VMAX, step 21117, the time delay pulse TVD is increased by the time step (T, step 21118, steps 21112 through 21117 are repeated to record additional counts in the eye data array 2111 at the appropriate time delay pulse TVD and variable voltage threshold VVT array positions. When the value of the time delay pulse TVD, step 21112, the measurement algorithm is at an end, step 21119. Typically, the measurement may be repeated many times to determine the quality of a high speed binary pulse bit stream. Thus, when finished, the operation of the measurement algorithm has enabled processor 210, Fig. 2, to generate a first eye data array 2111 in memory 211 of the processor wherein the sampled pulse voltage level counts are recorded at array positions defined by ones of the variable voltage threshold levels VVT separated by the voltage step (V and at ones of the time delayed clock pulses TVD separated by the time step (T during the pulse periods. An example of an eye data array showing typical count data collected by the measuring algorithm of Fig. 3 is set forth in Fig.5 of the drawing wherein the count data is recorded at the array positions TVD, VVT wherein the time delay pulses TVD are separated by the time step (T and the variable voltage thresholds VVT are separated by the voltage step (V.

[0022] The control 21 processor 210, Fig.2, operating under control of a processing algorithm program stored in memory 211 enables the processor210 to generate a second eye data array 2112 in memory 211. Processor 210, again under control of processing algorithm, processes the raw count data recorded in eye data array 2111 subtracting the pulse voltage count recorded in each time delay pulse TVD and voltage threshold VVT position plus one from the voltage threshold position VVT of each delayed clock pulse TVD and records the result as a count in a corresponding voltage threshold VVT and delayed clock position TVD of the second eye data array. The processor 210 displays the second eye data array 2112 as an eye diagram defining the characteristics and quality of the binary pulse bit stream.

[0023] The processing algorithm, Fig. 4, starts by having the user set the values of time TMAX, voltage VMAX, the time step (T, the voltage step (V and the minimum voltage VMIN, st p 21120. The valu of th time delay pulse TVD is then set to zero, step 21121. If the value of th time d lay puls TVD is qual to or less than the value of time TMAX, st p 21122, th value of variable voltage threshold VVT is s t equal to value of the minimum voltage VMIN, step 2123. When the value of the variable voltage threshold VVT is less than th valu of the maximum voltage VMAX, step 21124, an ey data array 2 position TVD, VVT is set equal to the absolute value of the count recorded in the eye data array position time delay pulse TVD and variable voltage threshold VVT +1 subtracted from the count recorded in the eye data array position time delay pulse TVD and variabl voltage threshold VVT. The variable voltage threshold VVT is increased by the value of the voltage step (V, step 21127 and the steps 21124 21124 through 1127 are repeated. When the value of the variable voltage threshold VVT is equal to the maximum voltage VMAX, step 21124, the value of the variable time delay pulse TVD is increased by (T and steps 21122 through 221124, 21126 and 21127 are repeated. The algorithm is completed when the value of the variable time delay pulse TVD is greater than the value of the maximum voltage TMAX. An example of the eye data array 2 2112 is set forth in Fig. 6 and has a count configuration off an ey diagram of the measured high speed binary pulse bit stream. Processor 210 is then enabled to display the processed count from eye data array2 2111 onto a display unit so that the eye diagram can be used to show the characteristics and quality of the measured binary pulse bit stream.

[0024] It is obvious from the foregoing that the facility, economy and efficiency of binary pulse coded waveform measuring apparatus has been improved by apparatus arrange to measure a high speed binary pulse bit stream and generate an eye diagram showing the characteristics and quality of the measured high speed binary pulse bit stream.

[0025] While the foregoing detailed description has described an embodiment of specific binary pulse coded waveform measuring apparatus, it is to be understood that the above description is illustrative only and is not limiting of the disclosed invention. Particularly other configurations are within the scope and sprit of this invention. Thus, the invention is to be limited only by the claims set forth below.

Claims

1. Apparatus for determining characteristics of a bit stream of binary pulses comprising

   measuring means for sampling pulse voltag levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream, and control means coupled to the measuring means for gen rating a s ries f the threshold voltage l v ls and th delayed clock pulses during each period of a bit stream puls and accumulating

multiple counts of the sampled pulse voltage lev ls during each delayed clock pulse for a series of pulses of the binary cod d puls bit stream and analyzing and processing the accumulated counts to generate an y diagram therefrom defining the characteristics of the binary pulse bit stream.

2. The binary pulse bit stream characteristics determining apparatus set forth in claim 1 wherein said control means comprises

a processor for determining a pulse repetition rate of the binary pulse bit stream and generating a series of the delayed clock pulses each separated by a predefined time step during a period of each binary pulse.

3. The binary pulse bit stream characteristics determining apparatus set forth in claim 2 wherein the processor generating a series of voltage threshold levels each separated by a predefined voltage step during each of the delayed clock pulses.

4. The binary pulse bit stream characteristics determining apparatus set forth in claim 3 wherein the processor generates a first eye data array in a memory of the processor wherein the sampled pulse voltage level counts are recorded at array positions defined by ones of the voltage threshold levels separated by the voltage step and at ones of the delayed clock pulses separated by the time step during the first pulse period.

5. The binary pulse bit stream characteristics determining apparatus set forth in claim 4 wherein the processor accumulates sampled pulse voltages counts in the eye data array at positions defined by the voltage threshold levels separated by the voltage step and at ones of the delayed clock pulses separated by the time step during pulse periods of the series of pulses succeeding the first pulse.

6. The binary pulse bit stream characteristics determining apparatus set forth in claim 5 wherein the processor generates a second eye data in the processor memory

7. The binary pulse bit stream characteristics determining apparatus set forth in claim 6 wherein the processor subtracts the pulse voltage count recorded in each voltage threshold position plus one of a delayed clock pulse from the voltage threshold position of each delayed clock pulse and records the result as a count in a corresponding voltage threshold and delayed clock position of the second eye data array.

8. The binary pulse bit stream characteristics det rmining apparatus set forth in claim 7 wher in the proc ssor displays th second y data array as th ye diagram defining the characteristics of the binary pulse bit stream.

9. A binary pulse waveform measuring apparatus for determining characteristics of a bit stream of binary pulses comprising

logic means for sampling pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream, and control means controlled by a program controlled processor and coupled to the logic means for generating a series of the threshold voltag levels and the delayed clock pulses during each period of a bit stream pulse and accumulating multiple counts of the sampled pulse voltage levels during each delayed clock pulse for a s - ries of pulses of the binary coded pulse bit stream and processing the accumulated counts to generate an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

10. The binary pulse waveform measuring apparatus set forth in claim 9 wherein the logic means comprise

a voltage comparator having a one pin input for receiving the bit stream of binary pulses and another comparison input for receiving a series of the voltage threshold levels each separated by a predetermined voltage step, and
a logic device having one input connected to an output of the voltage comparator for generating counts when the pulse voltage level exceeds the voltage threshold levels at each delayed clock pulse.

11. A binary pulse waveform measuring apparatus for determining characteristics of a bit stream of binary pulses comprising

logic means for sampling pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream, and control means controlled by a program controlled processor and coupled to the logic means for generating a series of the threshold voltag levels each separated by a predetermined voltage step and the delayed clock pulses each separated by a predetermined time step during each p riod of a bit stream pulse and accumulating multiple counts of the sampl d puls voltage l vels during ach d layed clock pulse for

a series of pulses of the binary coded pulse bit stream and processing the accumulated counts to generate an y diagram therefrom defining the characteristics of the binary pulse bit stream.

12. A method for determining characteristics of a bit stream of binary pulses comprising the steps of

generating a series of threshold voltage levels and delayed clock pulses during each period of a bit stream pulse,
measuring and accumulating multiple counts of pulse voltage levels in excess of the generated voltage threshold levels during each delayed clock pulse for a series of pulses of the binary coded pulse bit stream, and
analyzing and processing the accumulated voltage counts and generating an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

13. A method for determining characteristics of a bit stream of binary pulses comprising the steps of

sampling pulse voltage levels in excess of voltage threshold levels during each of delayed clock pulses for a series of pulses of the binary coded pulse bit stream,
generating a series of the threshold voltage levels and the delayed clock pulses during each period of a bit stream pulse and accumulating multiple counts of the sampled pulse voltage levels during each delayed clock pulse for a series of pulses of the binary coded pulse bit stream , and
processing the accumulated counts to generate an eye diagram therefrom defining the characteristics of the binary pulse bit stream.

14. The method for determining characteristics of a binary pulse bit stream set forth in claim 13 wherein the generating step comprises the step of

determining a pulse repetition rate of the binary pulse bit stream and generating a series of the delayed clock pulses each separated by a predefined time step during a period of each binary pulse.

15. The method for determining characteristics of a binary pulse bit stream set forth in claim 14 wherein the generating step further comprises the step of

generating a series of voltage threshold levels each separated by a predefined voltage step during each of the delayed clock pulses.

16. The method for determining charact ristics of a binary puls bit stream set forth in claim 14 wherein the generating step also comprises the step of

g nerating a first y data array in a memory of a processor wherein the sampled pulse voltage counts are recorded at array positions defined by on s of th voltage thr shold l vels separated by the voltage step and at ones of the delayed clock pulses separated by the time step during the first pulse period.

17. The method for determining characteristics of a binary pulse bit stream set forth in claim 14 wherein the processing step comprises the step of

generating a second eye data array in the processor memory.

18. The method for determining characteristics of a binary pulse bit stream set forth in claim 14 wherein the processing step further comprises the step of

subtracting the pulse voltage count recorded in each voltage threshold position plus one of a delayed clock pulse from the voltage threshold position of each delayed clock pulse and records the result as a count in a corresponding voltage threshold and delayed clock position of the second ey data array.

19. The method for determining characteristics of a binary pulse bit stream set forth in claim 14 wherein the processing step also comprises the step of

displaying the second eye data array as the eye diagram.

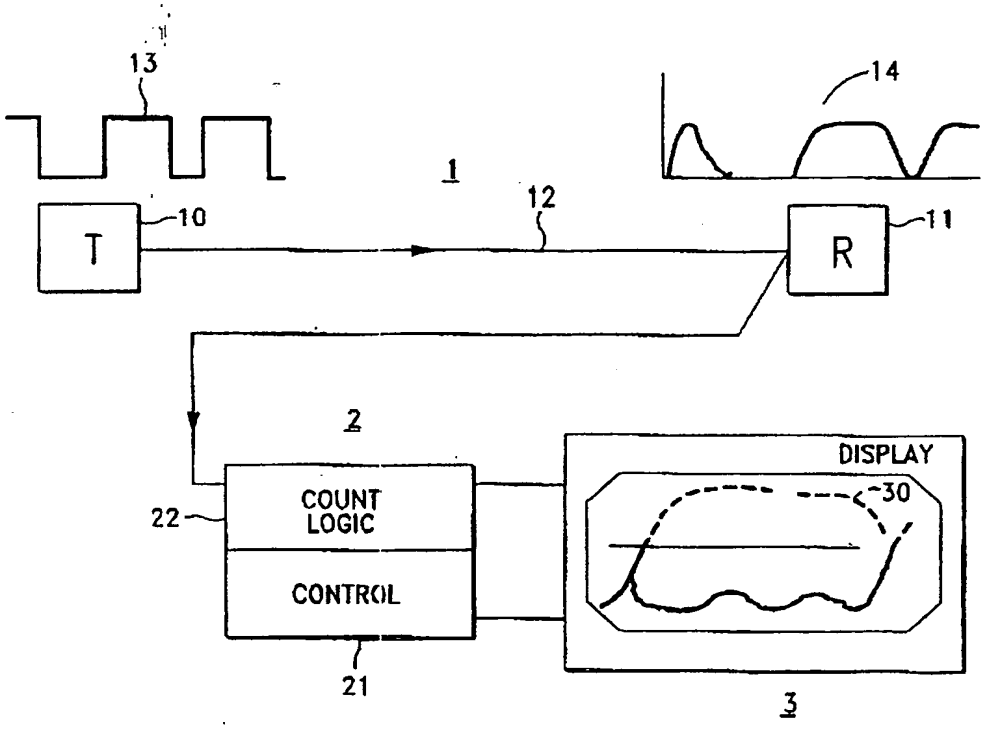

FIG.—1

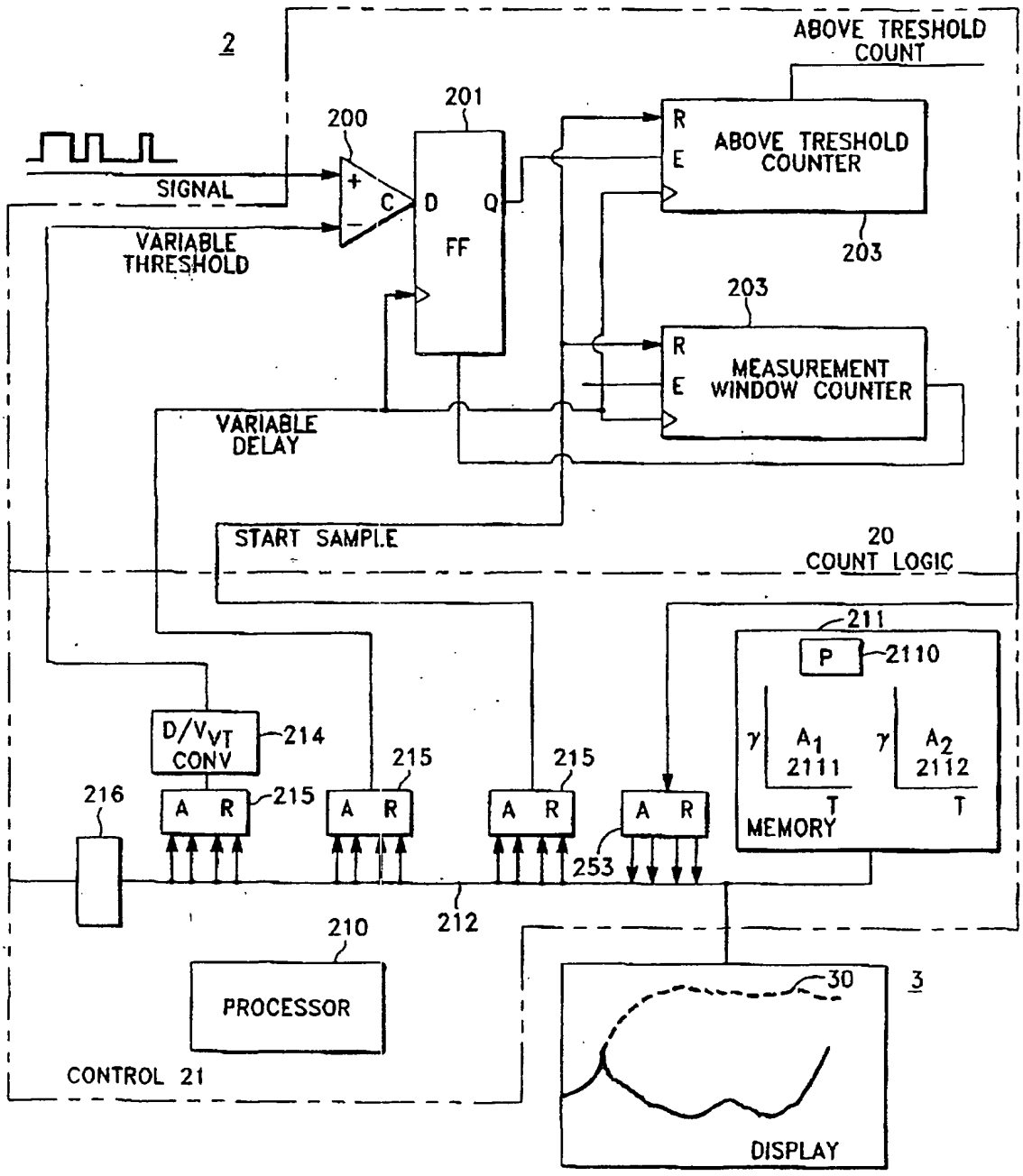
2
ABOVE TRESHOLD COUNT
201
200
SIGNAL
VARIABLE THRESHOLD
D
Q
FF
R
E
ABOVE TRESHOLD COUNTER
203
203
MEASUREMENT WINDOW COUNTER
VARIABLE DELAY
START SAMPLE
20
COUNT LOGIC
211
P
2110
D/V$_{VT}$ CONV
214
215
215
215
216
A R
A R
A R
A R
253
212
γ A$_1$ 2111 T
γ A$_2$ 2112 T
MEMORY
210
PROCESSOR
CONTROL 21
30
3
DISPLAY

FIG.—2

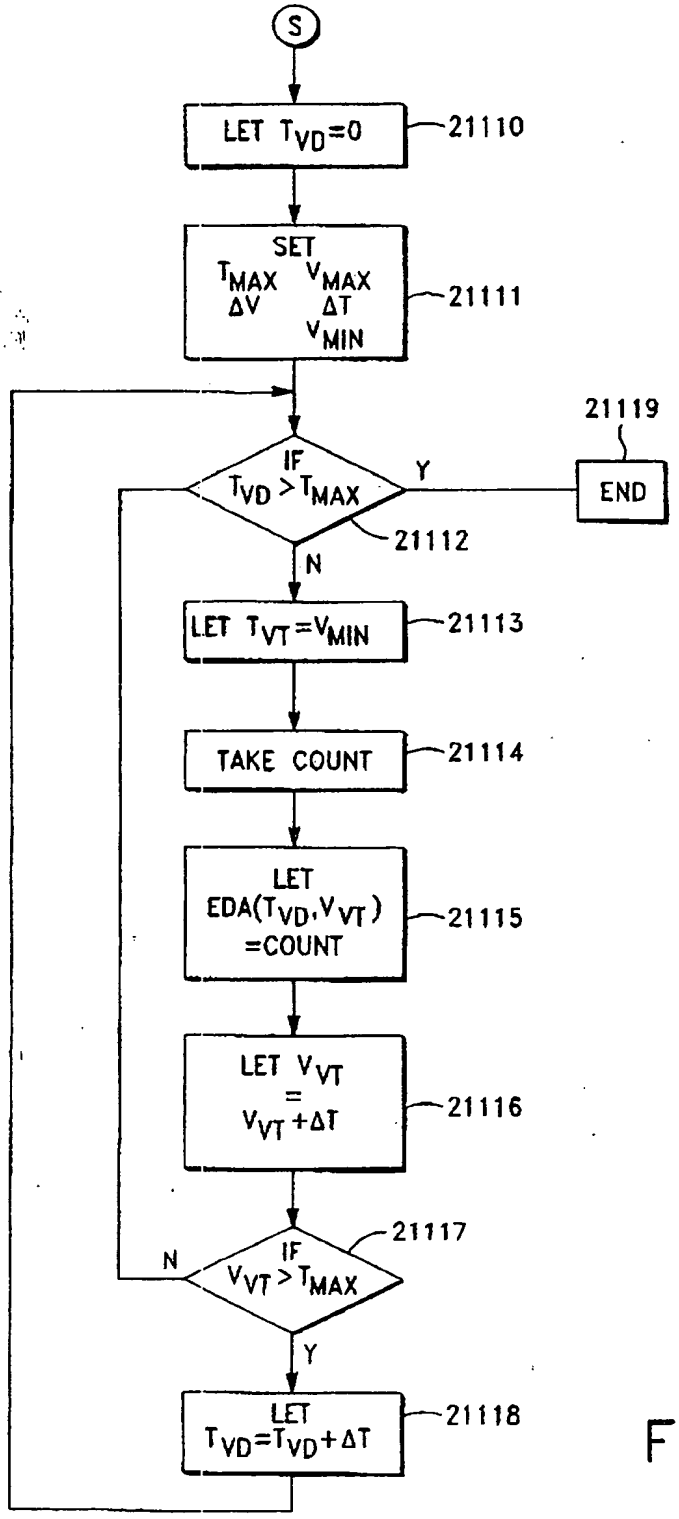
S
LET T_{VD}=0
21110
SET
T_{MAX} V_{MAX}
ΔV ΔT
V_{MIN}
21111
21119
IF
$T_{VD} > T_{MAX}$
Y
END
21112
N
LET T_{VT}=V_{MIN}
21113
TAKE COUNT
21114
LET
EDA(T_{VD},V_{VT})
=COUNT
21115
LET V_{VT}
=
V_{VT}+ΔT
21116
21117
IF
$V_{VT} > T_{MAX}$
N
Y
LET
T_{VD}=T_{VD}+ΔT
21118

FIG.—3

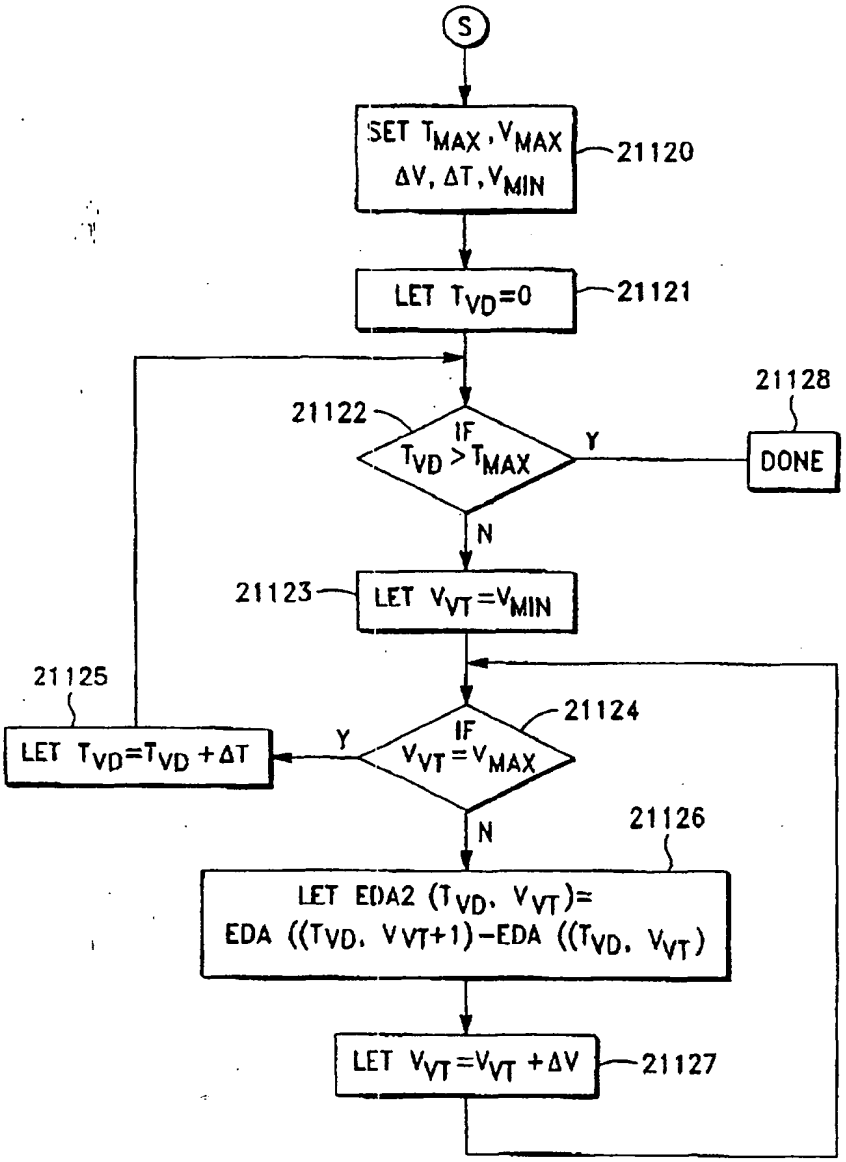
S
SET T_{MAX}, V_{MAX} ΔV, ΔT, V_{MIN}
21120
LET T_{VD}=0
21121
21122
IF $T_{VD} > T_{MAX}$
Y
21128
DONE
N
21123
LET V_{VT}=V_{MIN}
21125
LET T_{VD}=T_{VD} +ΔT
Y
21124
IF $V_{VT} = V_{MAX}$
N
21126
LET EDA2 (T_{VD}, V_{VT})= EDA ((T_{VD}, V_{VT}+1)−EDA ((T_{VD}, V_{VT})
LET V_{VT}=V_{VT} +ΔV
21127

FIG.—4

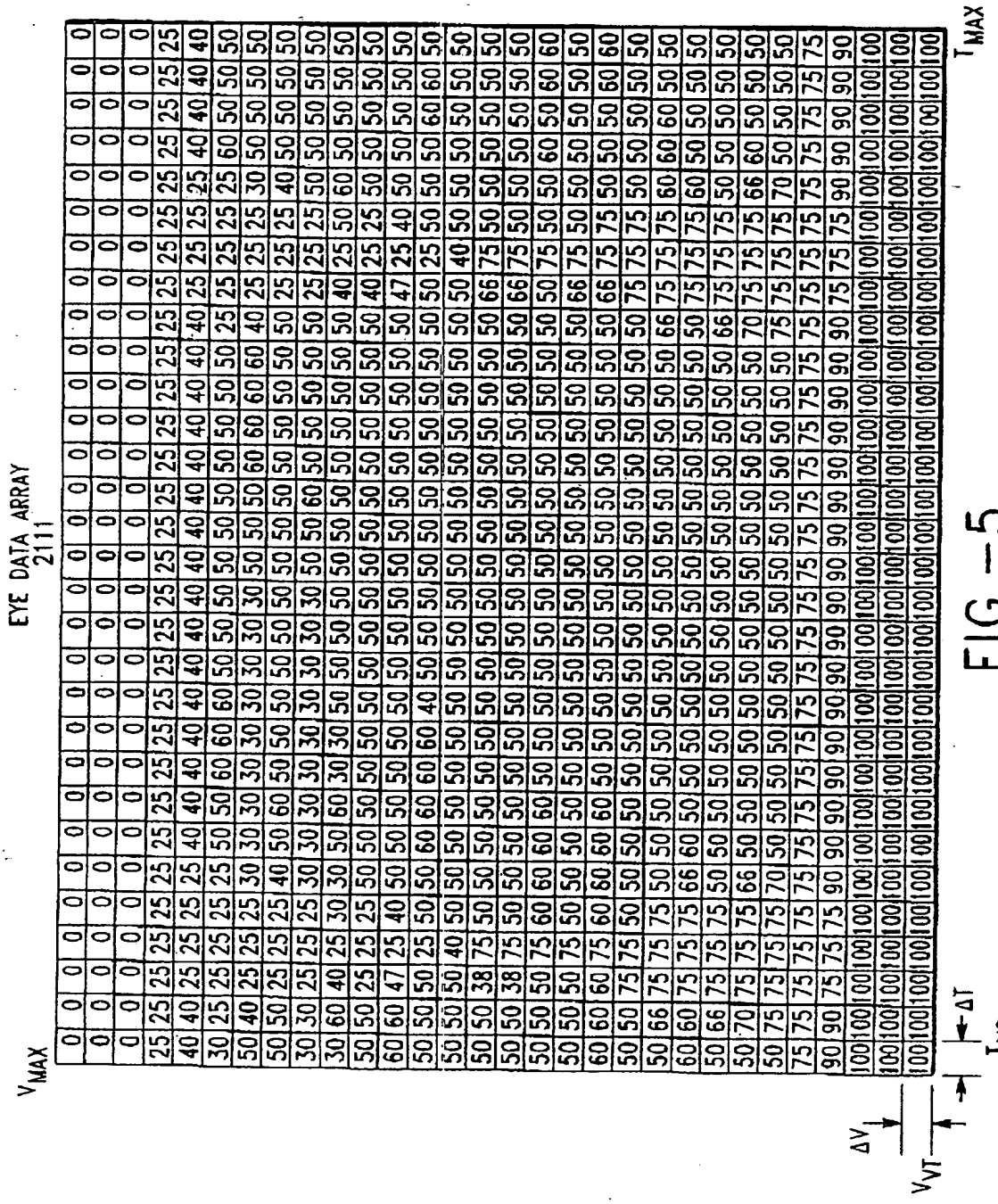

FIG.-5

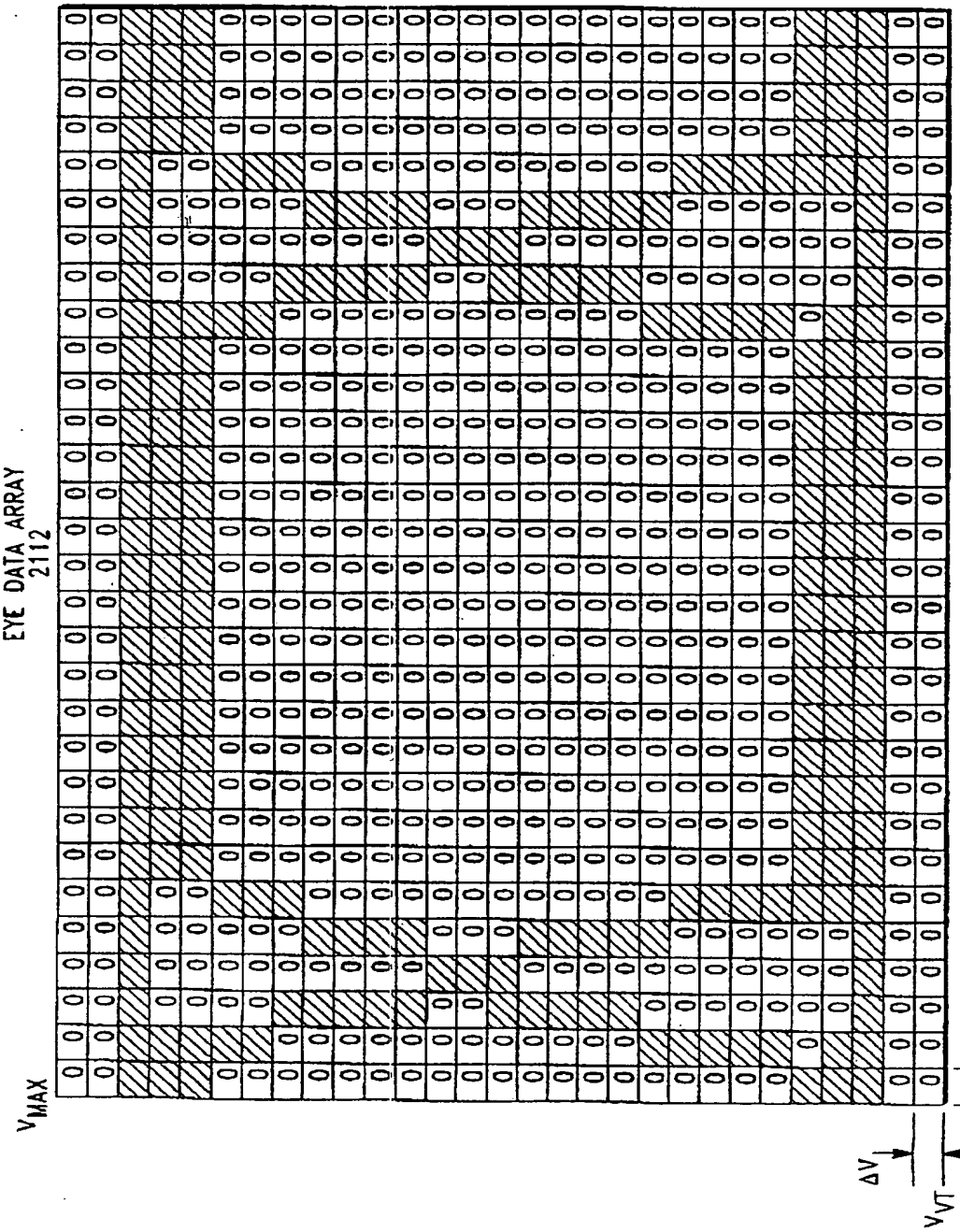

FIG.-6